AMENDMENTS TO THE DRAWINGS:

The attached sheets of drawings include changes to FIGURE 2, as indicated in red ink on the enclosed annotated sheets. These sheets, which include FIGURES 1-4, replace the prior amended sheets, which included FIGURES 1-4.

Attachments: Two Replacement Sheets

Annotated Sheet Showing Changes to FIGURE 2

REMARKS

The Applicant thanks the Examiner for the careful examination of this application and respectfully requests the entry of the amendments indicated hereinabove.

Claims 1-29 are pending and rejected. Claims 1, 14, and 24 are amended hereinabove. In response to the drawing objections and the 35 U.S.C. §112 rejections, FIGURE 2 has been amended. Regarding the fact that "VDD in Fig. 2 is not seen in Fig. 4 and Vpwell OR SUBSTRATE in Fig. 4 is not seen in Fig. 2" (page 3 of the Office Action), the Applicant notes that figures 2 and 4 are different parts of an SRAM device. Namely, FIG. 2 is peripheral circuitry that supplies V_{ADD} to the cell array (i.e. element 140 of FIG. 1) and FIG. 4 is the SRAM cell (i.e. element 115 of FIG. 1).

The Applicant is confused by the 35 U.S.C. §112, second paragraph rejections. The term "relative" is a term that is widely used and well understood by one of ordinary skill in the art. Furthermore, the term "relative" is used throughout the Specification and its meaning is clear from the reading of the Specification. Moreover, a change to the term "relative" to a different term within the Claims would mean that the Applicant would be using a claim term that does not match the wording of the Specification. The Applicant notes that in the field of electrical

engineering that all voltages are specified "relative" to some other voltage (often times its ground); therefore, no voltage is an absolute. For example, if voltage A is specified "relative" to voltage B, then whenever voltage B changes (up or down) that change is mimicked (up or down, respectively) by voltage A.

Regarding the rejection of Claims 2 and 15 on page 3 of the Office Action, the relationship between V_{ADD} and V_{well} is explained in paragraph 0040. The "how" is shown by the example circuit configuration of FIG. 2.

Regarding the rejection of Claim 3 on page 4 of the Office Action, the relationship between V_{ASS} and the substrate voltage is explained in paragraphs 0025, 0027, 0029, and 0040. The "how" is shown by the example circuit configuration of FIG. 2.

Regarding the rejection of Claims 4 and 16 on page 4 of the Office Action, the "how" is shown by the example circuit configuration of FIG. 2 and is explained in paragraph 0041.

Regarding the rejection of Claims 5-6 and 17-18 on page 4 of the Office Action, examples of the term "transistor parameters" is given in paragraphs 0029-0030, 0037 and 0040.

Regarding the rejection of Claims 7 and 19 on page 4 of the Office Action, the "how" is shown by the example circuit configuration of FIG. 2 and is explained in paragraphs 0027 and 0043. The Applicant notes that FIG. 2 is "an embodiment of a sleep mode voltage controller" that is "constructed according to the principles of the present invention" (paragraph 0032). Moreover, the Applicant notes that the controller may use any combination of fuses, transistors, diodes, ROM, or LDO, as explained in paragraph 0043. Therefore, the Applicant respectfully traverses the statement in the Office Action (page 4) that the sleep mode voltage controller "must" comprise the example shown in FIG. 2. The Applicant submits that he is not limited only to the FIG. 2 example circuit, rather "those skilled in the art should understand that they can make various changes, substitutions and alterations...without departing from the spirit and scope of the invention in its broadest form" (paragraph 0045).

Regarding the rejection of Claims 8 and 20 on page 4 of the Office Action, examples of optimizing values for a general technology class of transistors is given in paragraph 0030.

Regarding the rejection of Claims 9 and 21 on page 4 of the Office Action, the adjustment of V_{ADD} and V_{ASS} is explained in paragraphs 0031 and 0042 (see also FIG. 3). The "how" is shown by the example circuit configuration of FIG. 2.

Regarding the rejection of Claims 10 and 22 on page 4 of the Office Action, the adjustment of V_{ADD} and V_{ASS} is explained in paragraph 0031 and 0043 (see also FIG. 3). The "how" is shown by the example circuit configuration of FIG. 2.

Regarding the rejection of Claims 11 and 23 on page 5 of the Office Action, the "how" is shown by the example circuit configuration of FIG. 2 and explained in paragraph 0030. The Applicant notes that each voltage is not relative to a common reference, rather they are determined by a voltage difference. The Applicant also notes that the n-channel back bias voltage, the p-channel back bias voltage, and the voltage across the cell can all be made about the same voltage when the n-channel back bias voltage is a voltage between the substrate and the source of the n-channel transistor and the p-channel back bias voltage is a voltage between the nwell and the source of the p-channel transistor (see paragraph 0030).

Regarding the rejection of Claims 12-13 on page 5 of the Office Action, an explanation of a voltage that is sufficient for data retention is given in paragraphs 0006, 0025, and 0043.

Regarding the rejection of Claims 28-29 on page 5 of the Office Action, the Applicant notes that all voltages are specified "relative" to some other voltage

(often times its ground); therefore, no voltage is an absolute. Claims 28-29 are supported by paragraph 0025 on page 13 and paragraph 0035.

Independent Claim 1 positively recites a sleep mode voltage controller configured to provide both an array high supply voltage V_{ADD} that is lower than a high operating voltage V_{DD} and an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to the SRAM array during a sleep mode. Independent Claim 1 also positively recites that the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} are provided concurrently. These advantageously claimed features are not taught or suggested by the patent granted to Andersen et al.

Andersen et al. teaches away from the advantageously claimed invention because Andersen et al. teaches that the high voltage is allowed to float to a lower level (column 6 lines 5-9 and 44-54, column 7 lines 26-32 and 55-67, column 8 lines 1-4 and 42-46) and does not teach a controller that provides an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to the SRAM array during a sleep mode as advantageously claimed (FIG. 11A). The Applicant respectfully traverses the assertion in the Office Action (pages 5-6) that Andersen et al. discloses "a low-level of 0.3V higher than low operating voltage ground during a sleep mode". The Applicant submits that Andersen et al. discloses keeping the low power supply voltage constant at zero volts (FIG. 11A). The "high

level internal power supply voltage" and the "low-level power supply voltage" shown in FIG. 8 of Andersen et al. are merely the bounds within which only the high cell voltage (i.e. the internal V_{dd}) is to be maintained by the power management circuit (column 7 line 39 through column 8 line 4). Moreover, Anderson et al. does not teach or suggest providing V_{ADD} and V_{ASS} concurrently, as advantageously claimed (column 5 lines 38-41 and 44-46, column 6 lines 1-9 and 44-54, column 7 lines 39-45 and 55-67, column 8 lines 1-4, FIGS. 5-10).

Due to the foregoing reasons, the Applicant respectfully traverses the Examiner's rejection of Claim 1 and respectfully asserts that Claim 1 is patentable over Andersen et al. Furthermore, Claims 2-13 are allowable for depending on allowable independent Claim 1 and, in combination, including limitations not taught or described in the reference of record.

Independent Claim 14 positively recites providing both an array high supply voltage V_{ADD} that is lower than a high operating voltage V_{DD} and an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to the SRAM array during a sleep mode. Independent Claim 14 also positively recites that the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} are provided concurrently. These advantageously claimed features are not taught or suggested by the patent granted to Andersen et al.

Andersen et al. teaches away from the advantageously claimed invention because Andersen et al. teaches that the high voltage is allowed to float to a lower level (column 6 lines 5-9 and 44-54, column 7 lines 26-32 and 55-67, column 8 lines 1-4 and 42-46) and does not teach a controller that provides an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to the SRAM array during a sleep mode as advantageously claimed (FIG. 11A). The Applicant respectfully traverses the assertion in the Office Action (pages 5-6) that Andersen et al. discloses "a low-level of 0.3V higher than low operating voltage ground during a sleep mode". The Applicant submits that Andersen et al. discloses keeping the low power supply voltage constant at zero volts (FIG. 11A). The "high level internal power supply voltage" and the "low-level power supply voltage" shown in FIG. 8 of Andersen et al. are merely the bounds within which only the high cell voltage (i.e. the internal V_{dd}) is to be maintained by the power management circuit (column 7 line 39 through column 8 line 4). Moreover, Anderson et al. does not teach or suggest providing V_{ADD} and V_{ASS} concurrently, as advantageously claimed (column 5 lines 38-41 and 44-46, column 6 lines 1-9 and 44-54, column 7 lines 39-45 and 55-67, column 8 lines 1-4, FIGS. 5-10).

Due to the foregoing reasons, the Applicant respectfully traverses the Examiner's rejection of Claim 14 and respectfully asserts that Claim 14 is patentable over Andersen et al. Furthermore, Claims 15-23 are allowable for

depending on allowable independent Claim 14 and, in combination, including limitations not taught or described in the reference of record.

Independent Claim 24 positively recites modifying the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} during transition from an active mode to the sleep mode. Independent Claim 1 also positively recites that the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} are provided concurrently. These advantageously claimed features are not taught or suggested by the patent granted to Andersen et al.

Andersen et al. teaches away from the advantageously claimed invention because Andersen et al. teaches that the high voltage is allowed to float to a lower level (column 6 lines 5-9 and 44-54, column 7 lines 26-32 and 55-67, column 8 lines 1-4 and 42-46) and does not teach a controller that provides an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to the SRAM array during a sleep mode as advantageously claimed (FIG. 11A). The Applicant respectfully traverses the assertion in the Office Action (pages 5-6) that Andersen et al. discloses "a low-level of 0.3V higher than low operating voltage ground during a sleep mode". The Applicant submits that Andersen et al. discloses keeping the low power supply voltage constant at zero volts (FIG. 11A). The "high level internal power supply voltage" and the "low-level power supply voltage" shown in FIG. 8 of Andersen et al. are merely the bounds within which only the

high cell voltage (i.e. the internal V_{dd}) is to be maintained by the power management circuit (column 7 line 39 through column 8 line 4). Moreover, Anderson et al. does not teach or suggest providing V_{ADD} and V_{ASS} concurrently, as advantageously claimed (column 5 lines 38-41 and 44-46, column 6 lines 1-9 and 44-54, column 7 lines 39-45 and 55-67, column 8 lines 1-4, FIGS. 5-10).

Due to the foregoing reasons, the Applicant respectfully traverses the Examiner's rejection of Claim 24 and respectfully asserts that Claim 24 is patentable over Andersen et al. Furthermore, Claims 25-29 are allowable for depending on allowable independent Claim 24 and, in combination, including limitations not taught or described in the reference of record.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,

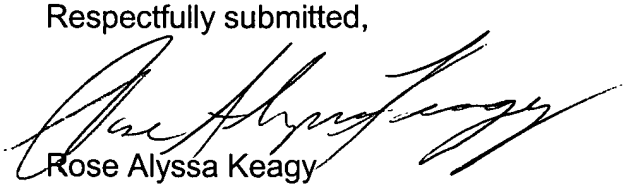

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FIG. 1

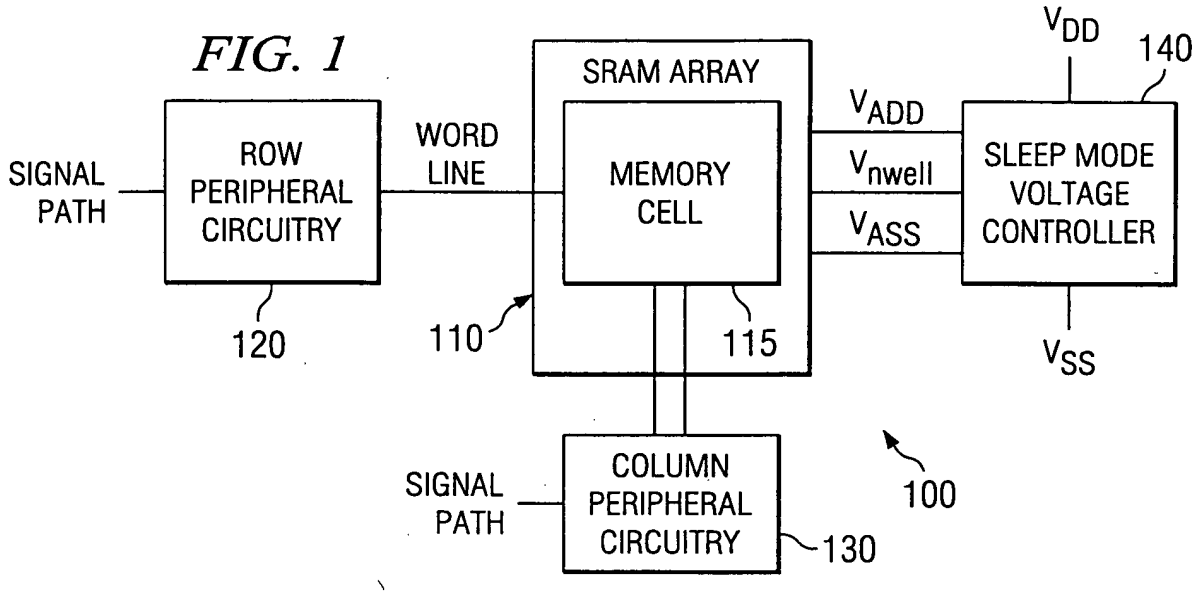

FIG. 2